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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/990,027 | 11/20/2001 | Jefferson Eugene Owen | 97-S-152D1 | 2782 |

30425 7590 09/29/2004

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|---|---|
| LE, VU | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2613 | |

DATE MAILED: 09/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/990,027 | OWEN ET AL. | |
| | Examiner | Art Unit | |
| | Vu Le | 2613 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *16-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-19* is/are allowed.

6)☒ Claim(s) *16,20-25,27-30 and 33-35* is/are rejected.

7)☒ Claim(s) *26,31 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6-11-02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, *except* that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English.

2. Claims 16, 20-21, 29-30, 33-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Malladi et al, US 5,903,312.

Re claim 16, Malladi et al discloses a method for providing video motion compensation (fig. 2, col. 13, line 46 to col. 15, line 44) comprising the steps of:

receiving one or more prediction blocks (fig. 3A is the exploded illustration of "160" in fig. 2, and fig. 3B is the exploded illustration of "158" in fig. 2, as shown in both figures, prediction blocks are "186" i.e. DCT Coeff.);

receiving one or more instructions (fig. 2: 164 & 165, col. 15, lines 34-44);

receiving one or more error terms (col. 15, lines 14-33);

and utilizing at least the one or more prediction blocks and the one or more error terms as directed by the one or more instructions to produce a decoded macroblock

(col. 14, lines 43-63, again, the DCT coefficients "186" represent one or more prediction blocks).

Re claim 20, Malladi et al discloses a system for providing video motion compensation (fig. 2, col. 13, line 46 to col. 15, line 44) comprising:

a video decoder configured to produce one or more instructions and one or more error terms (163-164 function integrally as a video decoder configured to produce decoding instruction via 164 and error terms via 163, see also col. 13, lines 39-49 and col. 14, lines 47-50, col. 15, lines 14-44);

a picture memory (181-183 store reference pictures);

and a digital video processor (164-165 & 174-183 integrally function as a digital video processor) comprising:

an error memory (174) communicably coupled to the video decoder (174 is coupled to 163 and 164 respectively);

a half pixel filter (176) communicably coupled to the picture memory (176 is communicably coupled to 181-183 via 185, 177);

a merge memory (174 also serves as merge memory) communicably coupled to the half pixel filter (174 is coupled to 176 via 178);

a controller (164 by itself functions as a controller) communicably coupled to the video decoder (coupled to 163 via 168), the error memory (directly coupled to 174), the merge memory (directly coupled to 174) and the half pixel filter (directly coupled to 176);

a sum unit (175 serves as the sum unit for picture reconstruction, col. 14, lines 51-55) communicably coupled to the error memory (directly coupled to 174), the merge memory (directly coupled to 174) and the picture memory (directly coupled to 180-183);

and the controller (164) executing the one or more instructions to provide motion compensation (col. 14, line 64 to col. 15, line 44, in this segment, the register 164 controls motion compensation of P and B macroblocks).

Re claim 21, the system for providing video motion compensation as recited in claim 20, further comprising: an error buffer communicably coupled between the error memory and the video decoder (172); an instruction buffer communicably coupled between the controller and the video decoder (168); a reference buffer communicably coupled between the half pixel filter and the picture memory (177); and a display buffer communicably coupled between the sum unit and the picture memory (180).

Re claim 29, the method as recited in claim 16, further comprising: receiving the one or more prediction blocks, the one or more instructions, and the one or more error terms from a video decoder capable of selectively formulating the instructions. (The limitations of claim 29 have been analyzed and rejected w/r to claim 16).

Re claim 30, the method as recited in claim 16, further comprising: filtering the one or more prediction blocks with a half pixel filter performing vertical and horizontal half-pixel interpolation on each prediction block as dictated by a motion vector within an instruction associated with the prediction block; and utilizing each of the one or more error terms with an associated filtered prediction block from the one or more prediction

blocks filtered by the half pixel filter to produce the decode macroblock. (See figs. 5A-5D, col. 23, line 26 to col. 24, line 57).

Re claim 33, the method as recited in claim 16, further comprising: storing the one or more received error terms within an error memory communicably coupled to a controller for executing the one or more instructions. (Claim 33 has been analyzed and rejected w/r to claim 20).

Re claim 34, the method as recited in claim 16, further comprising: filtering the one or more prediction blocks with a half pixel filter performing vertical and horizontal half-pixel interpolation on each prediction block as dictated by a motion vector within an instruction associated with the prediction block; and storing filtered prediction blocks within a merge memory communicably coupled to a controller for executing the one or more instructions. (Claim 34 has been analyzed and rejected w/r to claims 20 and 30).

Re claim 35, the method as recited in claim 16, further comprising: storing the one or more instructions within an instruction queue communicably coupled to a controller for executing the one or more instructions. (Claim 35 has been analyzed and rejected w/r to claim 20. Also, figure 2 of Malladi et al shows a register "REG" 165, which serves as an instruction queue coupled to the controller 164 as claimed).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Malladi et al.

Claim 22 recites "[T]"he system for providing video motion compensation as recited in claim 21, wherein the error memory, the merge memory, the picture memory, the error buffer, the instruction buffer, the display buffer and the reference buffer are static random access memory [.]" It is evidenced in Malladi et al that static RAM are utilized, for example the error buffer (172) and the instruction buffer (168) are static RAMs. Malladi et al does not extend the description of static RAM to the error memory, the merge memory, the picture memory, the display buffer and the reference buffer as claimed. Nevertheless, one skilled in the art would have found it obvious and reasonable to conclude that static RAM would qualify to serve as memory and buffering means as recited in claims 21-22 since using RAM is notoriously well known and beneficial for temporary storage.

5. Claims 23-25, 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (fig. 1 of the drawings) in view of Malladi et al.

Re claim 23, applicant's admitted prior art (fig. 1) shows a digital video system comprising:

DVD drive (32);

a track buffer communicably coupled to the DVD drive (34);

a demultiplexer communicably coupled to the track buffer (36);

a video input buffer communicably coupled to the demultiplexer (44);

a digital video decoder (54) communicably coupled to the video input buffer (44), the digital video decoder (54) utilizing at least an encoded video data stream to produce one or more output streams, the one or more output streams comprising at least a set of motion compensation instructions and a set of error terms (page 15, lines 7-11, in this segment, the encoded video data is an MPEG bitstream, thus motion compensation instructions are implicitly taught), and a mixer (74) communicably coupled to the video decoder.

Applicant's admitted prior art fails to further teach a digital video processor coupled to the digital video decoder, the digital video processor providing motion compensation using the set of motion compensation instructions and the set of error terms; the digital video processor is then coupled to the mixer, and a video renderer communicably coupled to the mixer as claimed.

Malladi et al discloses a computer system that serves as a digital video system (figs. 1B-1C & 2, also col. 7, lines 13-36). The computer system reads program instructions for video decoding from various media including optically readable media. Thus, a drive to read the optical media is implicitly taught (see col. 7, lines 26-36). The computer video system of Malladi et al is illustratively represented in figures 1B-1C and fig. 2. Figure 1C shows a subset of the computer video system that includes digital video decoder ("VIDEO CORE") communicably coupled to the a digital video processor ("MACROBLOCK PROCESSING LOGIC"). As shown in figure 1C, the video processor providing motion compensation using the set of motion compensation instructions and the set of error terms (126,136, col. 10, lines 36-59, col. 11, lines 17-52). The motion

compensation instructions and the error terms are then "rendered" at the merge operation (134, col. 11, lines 46-52).

Therefore, taking the combined teaching of applicant's admitted prior art and Malladi et al as a whole, it would have been obvious to modify the prior art digital video system in view of Malladi et al to also include a digital video processor coupled to the digital video decoder, wherein the digital video processor providing motion compensation using the set of motion compensation instructions and the set of error terms, and wherein the digital video processor is then coupled to the mixer, and a video renderer (merge operation) communicably coupled to the mixer as claimed, for the benefit of having reusable hardware layout ("core") for performing some, but not all, MPEG-2 video decoding functions. The functional blocks comprising this "video core" define a unique hardware architecture which can be used with additional hardware or software for performing those MPEG-2 video decoding functions not performed by the video core as (Malladi et al, col. 2, line 64 to col. 3, line 3).

Re claim 24, the digital video system as recited in claim 23, wherein the digital video processor further comprises: an error memory and a merge memory; a half pixel filter communicably coupled to the merge memory; a controller communicably coupled to the error memory, the merge memory and the half pixel filter, the controller executing the motion compensation instructions; and a sum unit communicably coupled to the error memory and the merge memory. (The limitations of claim 24 would have been obvious to incorporate by the combined teaching of applicant's admitted prior art in view

of Malladi et al w/r to claim 20, which has been analyzed and rejected. The motivation to combine has been analyzed and explained w/r to claim 23).

Re claim 25, the digital video system as recited in claim 24, wherein the digital video processor further comprises: an error buffer communicably coupled to the error memory; an instruction buffer communicably coupled to the controller; a reference buffer communicably coupled to the half pixel filter; and a display buffer communicably coupled to the sum unit. (The limitations of claim 25 would have been obvious to incorporate by the combined teaching of applicant's admitted prior art in view of Malladi et al w/r to claim 21, which has been analyzed and rejected. The motivation to combine has been analyzed and explained w/r to claim 23).

Re claim 27, the digital video system as recited in claim 24, wherein the sum unit uses at least one of the error terms stored in the error memory with one or more filtered prediction blocks stored in the merge memory to produce a decoded macroblock. (The limitations of claim 27 would have been obvious to incorporate by the combined teaching of applicant's admitted prior art in view of Malladi et al with respect to claims 20 and 21, which have been analyzed and rejected. Furthermore, in fig. 2 of Malladi et al, the summing operation performed by the "RECON" 175 necessitates summing at least one of the error terms stored in the error memory with one or more filtered prediction blocks stored in the merge memory to produce a decoded macroblock. This is implied and necessitated. The motivation to combine has been analyzed and explained w/r to claim 23).

Re claim 28, the digital video system as recited in claim 24, wherein the half pixel filter performs vertical and horizontal half-pixel interpolation on a block as dictated by a motion vector. (The limitations of claim 28 would have been obvious to incorporate by the combined teaching of applicant's admitted prior art in view of Malladi et al with respect to claims 20 and 21, which have been analyzed and rejected. Furthermore, in figs. 2 and 5B-5D of Malladi et al, the half pixel filter performs vertical and horizontal half-pixel interpolation on a block as dictated by a motion vector, see col. 24, lines 1-57. The motivation to combine has been analyzed and explained w/r to claim 23).

***Allowable Subject Matter***

6. Claims 26, 31-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 26 further recites "the controller further comprises: an instruction queue; an execution unit communicably connected to the instruction queue and the error memory; a motion compensation state machine communicably coupled to the execution unit, the half pixel filter and the merge memory[.]" The prior art of record fails to anticipate or render obvious the execution unit and the motion compensation state machine in the manner as claimed.

Claim 31 further recites "...the step of receiving one or more instructions further comprises: receiving at least one each motion compensation instruction comprising an instruction descriptor followed by one or more data descriptors, the instruction descriptor comprising at least a first data field and a second data field, the first data field

indicating an operation to be performed and the second data field indicating how many of the data descriptors follow the instruction descriptor, each data descriptor comprising a third data field and a fourth data field, the third data field indicating a memory address of a first word in a prediction block associated with the at least one motion compensation instruction and the fourth data field indicating a number of words in the prediction block[.]" The prior art of record fails to anticipate or render obvious the each motion compensation instruction comprising an instruction descriptor in the manner as claimed.

Claim 32 further recites "...further comprising: utilizing the one or more instructions to control a motion compensation state machine employed to produce the decoded macroblock[.]" The prior art of record fails to anticipate or render obvious the motion compensation state machine in the manner as claimed.

7. Claims 17-19 are allowed.

Claim 17 governs claims 18-19, and recites "[A] method for providing video motion compensation comprising the steps of: receiving an instruction and writing the instruction to an instruction queue; moving the instruction from the instruction queue to an execution unit if the execution unit is not full; receiving an error term and writing the error term to an error memory; executing the instruction in the execution unit if the instruction is not a write instruction; and if the instruction in the execution unit is a write instruction, waiting until the error memory is full, and then utilizing at least all the error terms stored in the error memory and one or more prediction blocks stored in a merge memory to produce a decoded macroblock[.]" The prior art of record fails to anticipate

or render obvious the method steps and relationship of between the instruction queue and the execution unit in the manner as claimed to achieve motion compensation.

***Response to Preliminary Amendment***

8. Claims 1-15 have been canceled.

## Contact

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vu Le whose telephone number is 703-308-6613. The examiner can normally be reached on M-F 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Kelley can be reached on 703-305-4856. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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